

LCFC CONFIDENTIAL

S145-IGM M/B FS440/FS541 Schematics Document

Intel Geminilake M-Processor with DDR4 + UMA

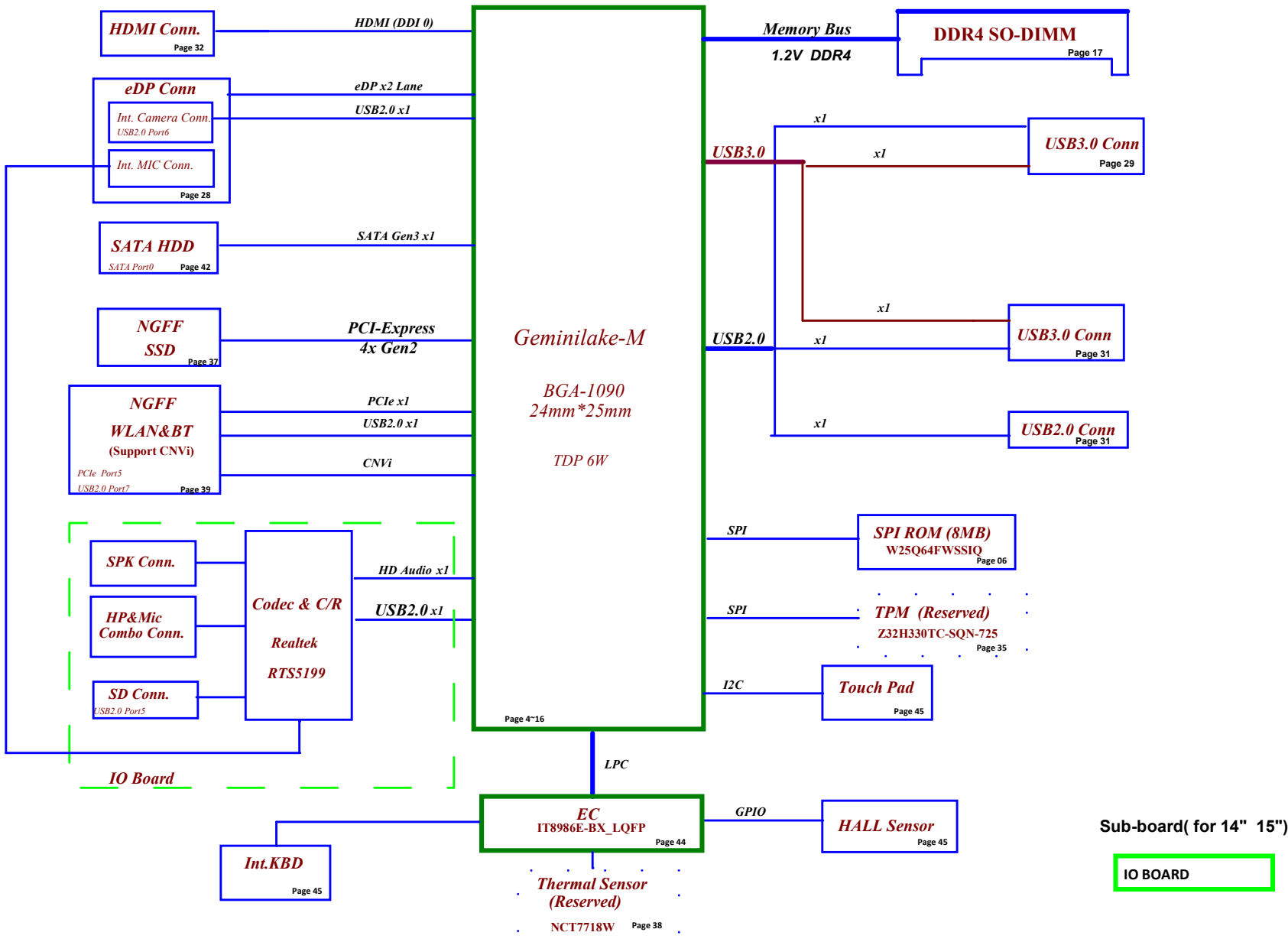
2018-07-09

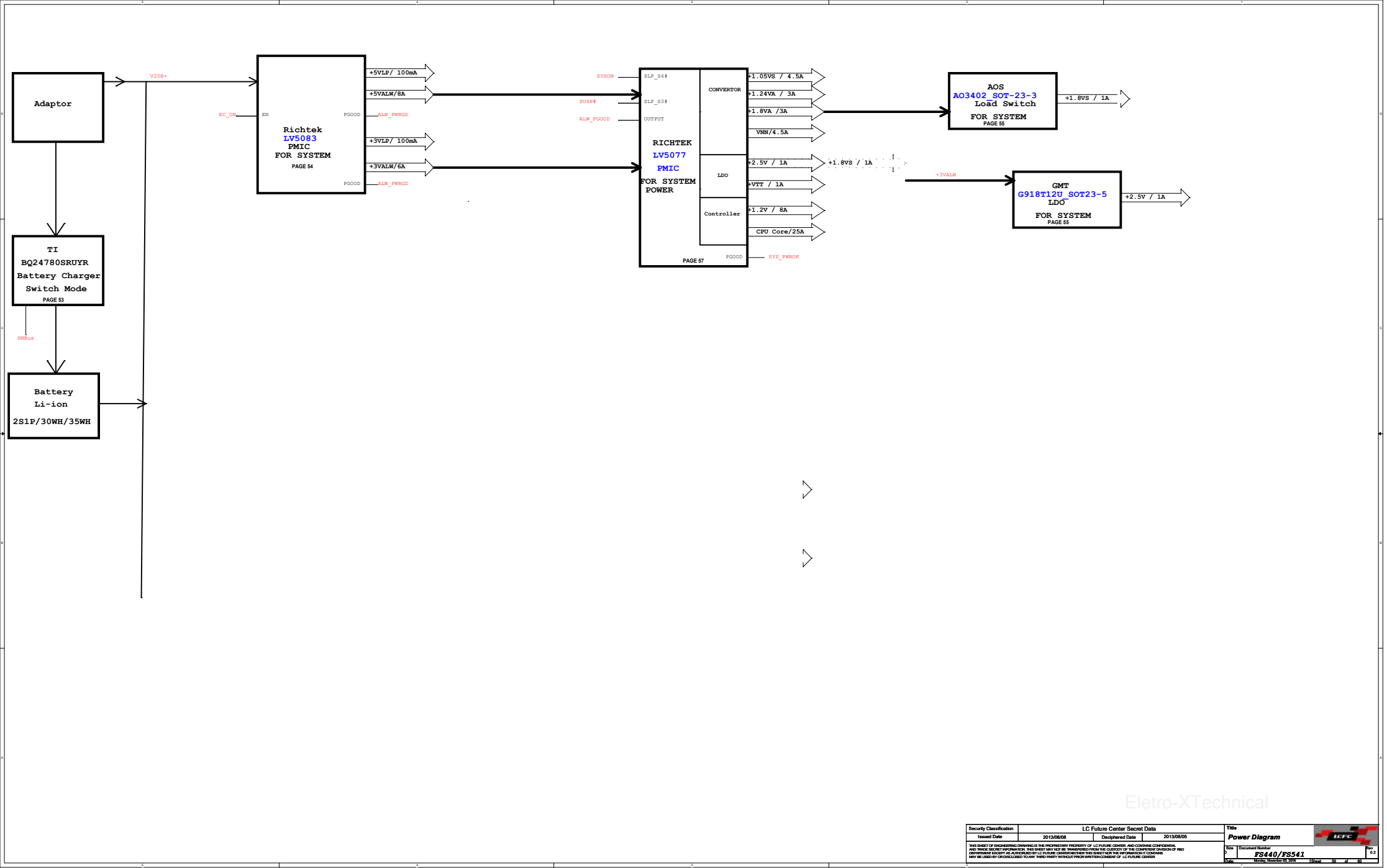
REV:1.0

Security Classification		LC Future Center Secret Data		7133	
Issued Date	2018/07/09	Deciphered Date	2019/07/08	Cover Page	
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Rev 0.2





Voltage Rails (0 --> Means ON , X --> Means OFF)

<div>Power Plane</div> <div>State</div>	V20B+ +3VL +5VL	+3VALW +5VALW	+3VALW_SOC +1.24VALW +1.8VALW	+1.2V	+5VS +3VS +1.8VS +1.05VS +0.6VS +CPU_CORE +VNN
S0	O	O	O	O	O
S3	O	O	O	O	X
S5 S4/AC Only	O	O	O	X	X
S5 S4 Battery only	O	X	X	X	X
S5 S4 AC & Battery don't exist	X	X	X	X	X

STATE \ SIGNAL	SLP_S0#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS/VTT	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S0IX(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	OFF
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

USB Port Table

XHCI	Port	Port device
USB 3.0	0	USB3.0
	1	USB3.0
USB 2.0	0	
	1	USB3.0 (2.0)
	2	BT
	3	USB3.0 (2.0)
	4	USB2.0
	5	CARD READER
	6	CAMERA
	7	Touch Screen(RSVD)

DDI PORT LIST

Port	Device
DDI0	HDMI
DDI1	NC
eDP	eDP

PCIE PORT LIST

Port	Device	BIOS Device ID Map	CLK REQ
0	dGPU	PCle1(Func0):Root Port#3	CLKREQ0
1			
2			
3			
4	LAN	PCle0(Func0):Root Port#1	CLKREQ1
5	WLAN	PCle0(Func1):Root Port#2	CLKREQ2

BOM Structure Table

BOM Structure	BTO Item
EMC@	For EMC part
EMC_NS@	For EMC un-stuff part
EMC_15@	EMC 15" part
14@	For 14" part
15@	For 15" part
RF@	For RF part
CD@	Cost Down part
DIS@	DIS SKU ID part
UMA@	UMA SKU ID part
IGM@	IGM CPU SKU part
IGMR@	IGMR CPU SKU part
LBG@	LBG project SKU part
NEC@	NEC project SKU part
CNVI@	CNVI SKU part
TMSen@	Thermal Sensor part
TMSen_UMA@	UMA Thermal Sensor part
TPM@	TPM part
Debug@	USB debug feature part
USB@	Non USB debug feature part
TS@	Touch Screen part
TS_LBG@	LBG project Touch Screen part
TS_NEC@	NEC project Touch Screen part
UART@	UART debug part
RTCRST@	Clear RTCRST# function part
ME@	ME part
@	un-stuff part
HDMI@	HDMI Logo part
N4100@	GLK N4100 CPU part
N4000@	GLK N4000 CPU part
N5000@	GLK N5000 CPU part
N4100_QS@	GLK N4100 QS CPU part
HDA18@	HDA Bus 1.8V power part
HDA33@	HDA Bus 3.3V power part
NM_C111@	MB PCB part
NS_C121@	ODD PCB part

SMBUS Control Table

	SOURCE	VGA	BATT	IT8986HE	SODIMM	WLAN WiMAX	Thermal Sensor	PCH	TP Module	Charger	PMIC
EC_SMB_CK0 EC_SMB_DA0	EC +3VL	X	X	V	X	X	X	X	X	X	V
EC_SMB_CK1 EC_SMB_DA1	EC +3VL	X	V	V +3VL	X	X	X	X	X	V	X
EC_SMB_CK2 EC_SMB_DA2	EC +3VS	X	X	V +3VS	X	X	V	X	X	X	X
PCH_SMB_CLK PCH_SMB_DATA	PCH +3VALW_SOC	X	X	X	V +3VS	V +3VS	X	V +3VALW_PCH	X	X	X

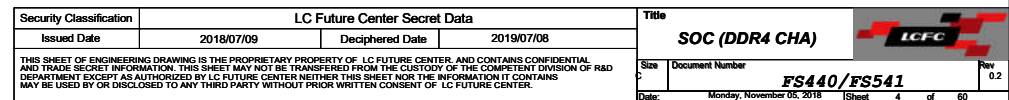
EC SM Bus0 address		EC SM Bus1 address		EC SM Bus2 address		PCH SM Bus address	
Device	Address	Device	Address	Device	Address	Device	Address
PMIC	0x68	Smart Battery	0x16	Thermal Sensor	0x38(reserve)	DDR SO-DIMM	0xA0
		Charger	0x12			Wlan	Rsvd

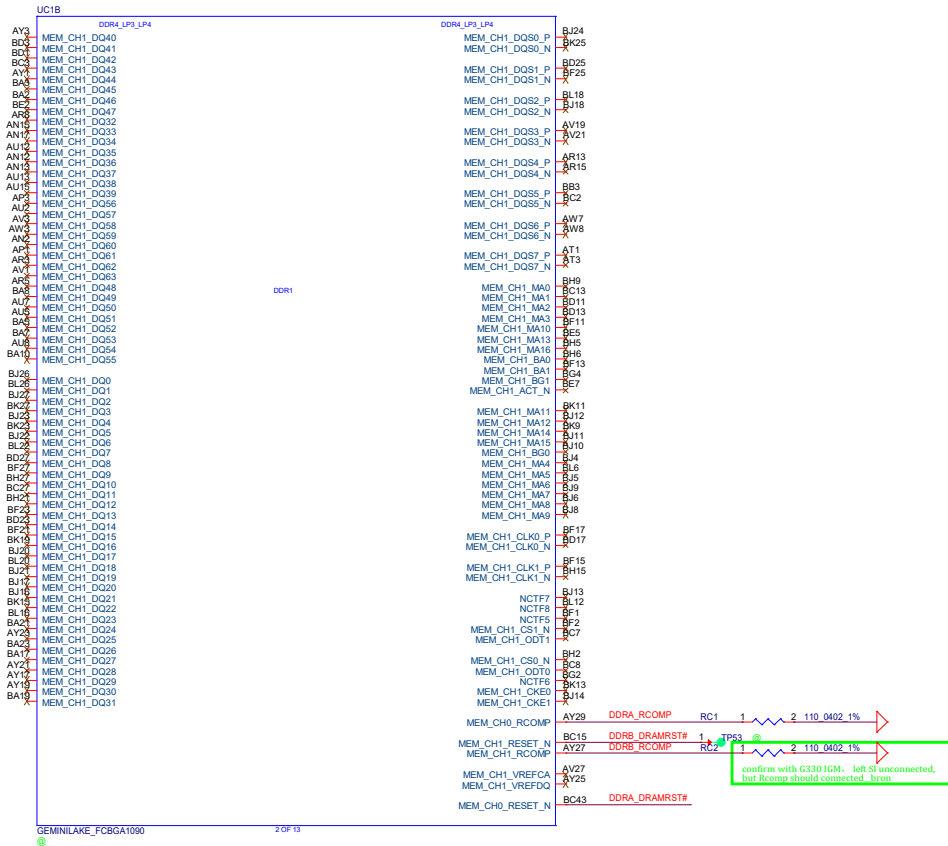
I2C4/I2C7 Bus address (Touch Pad)

Device	Address
Slave	0x15
Descriptor	0x0001

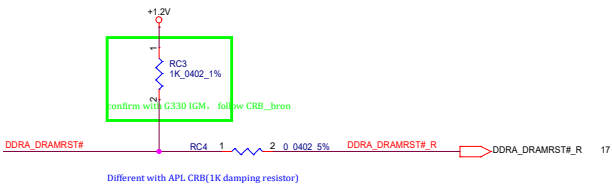
RCOMP RESISTOR REQUIREMENT

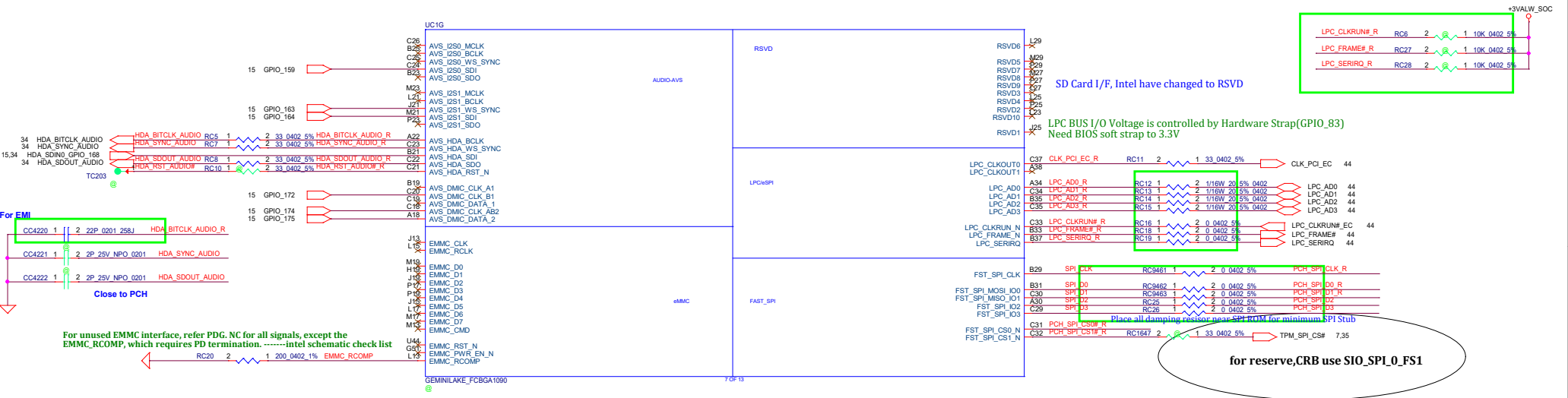
INTERFACE	PIN NAME	LOCATION	VALUE(ohm)
Memory	MEM_CH0_RCOMP	RC1	110 +/-1%
	MEM_CH1_RCOMP	RC2	110 +/-1%
USB2	USB2_RCOMP	RC64	113 +/-1%
USB3/PCIE/SATA	PCIE2_USB3_SATA3_RCOMP_P/N	RC63	100 +/-1%
PCIE Refclk	PCIE_REF_CLK_RCOMP	RC62	56 +/-1%
DP/eDP*/HDMI*	EDP_RCOMP_P/N	RC79	100 +/-1%
MDSI	MDSI_RCOMP	RC78	150 +/-1%
CNVi	CNV_WT_RCOMP	RC48	150 +/-1%
SMBUS/GPIO/EMMC for all 1.8V only and 1.8V mode operation of 1.8/3.3V CFIO interfaces	EMMC_RCOMP	RC20	200 +/-1%



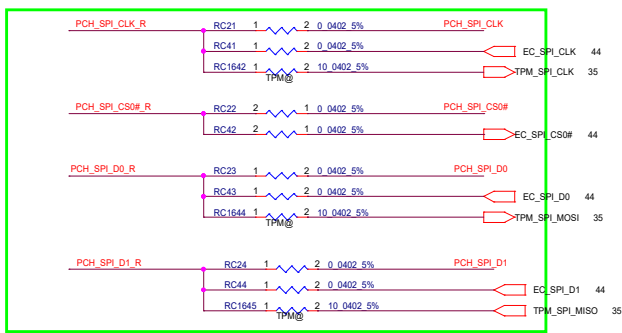


Follow CRB&PDG v1.2

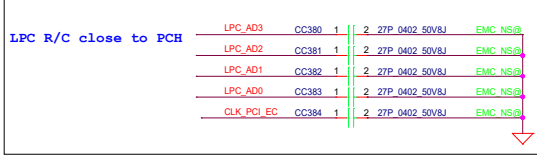
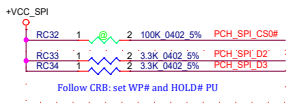




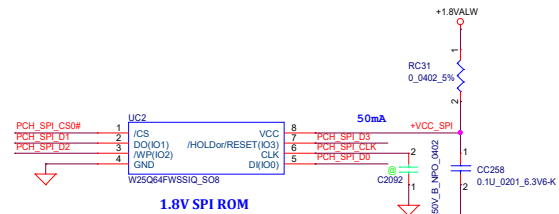
SPI ROM



Near place RC21&RC41; RC22&42; RC23&RC43; RC24&RC44



Ball Name	Signal Name	I/O Voltage	Default Term	Buffer Type
FST_SPI_CS0_N	PCH_SPI_CS0#	1.8V	Native	HSMV
FST_SPI_MOSI_I00	PCH_SPI_D0	1.8V	Native	HSMV
FST_SPI_MISO_I01	PCH_SPI_D1	1.8V	Native	HSMV
FST_SPI_I02	PCH_SPI_D2	1.8V	Native	HSMV
FST_SPI_I03	PCH_SPI_D3	1.8V	Native	HSMV
FST_SPI_CLK	PCH_SPI_CLK	1.8V	Native	HSMV



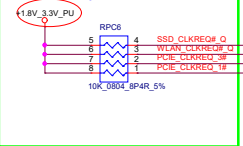
SSD

HDD

PCIE Configuration

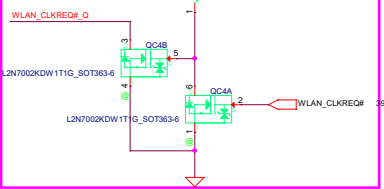
Port	Config	Device	Name:Dev:Fun:DID:Root Port
P0			
P1	X4	SSD	PCIe1(Func0):19:0:0x31D8:2
P2			
P3			
P4	X1		PCIe0(Func0):20:0:0x31D6:0
P5	X1	WLAN	PCIe0(Func1):20:1:0x31D7:1

CLOCK REQUEST

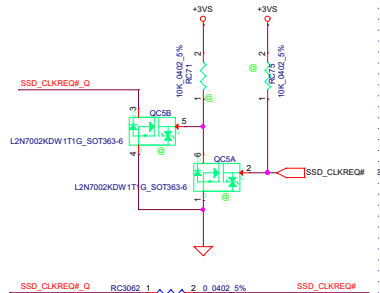


Need Check
CLKREQ# can be set 1.8V/3.3V by soft strap
CLKREQ0/2/4 default 3.3V
CLKREQ1 default 1.8V

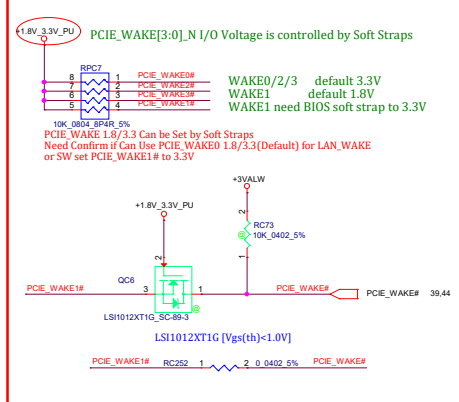
PCIE_CLKREQ[3:0]_N I/O Voltage is controlled by Soft Straps



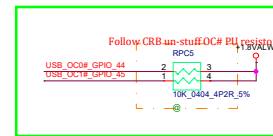
CLKREQ# can be set 1.8V/3.3V by soft strap

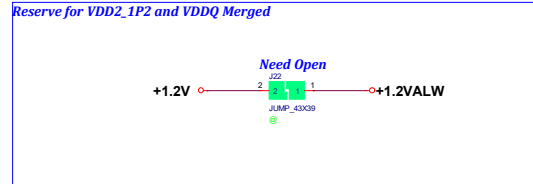
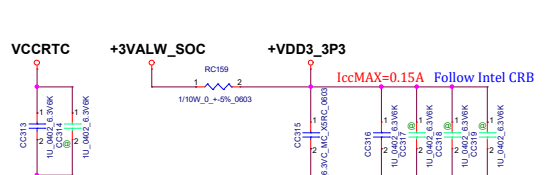
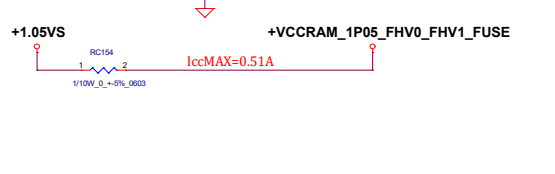
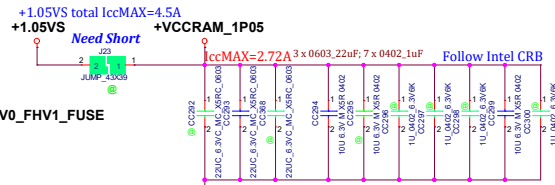
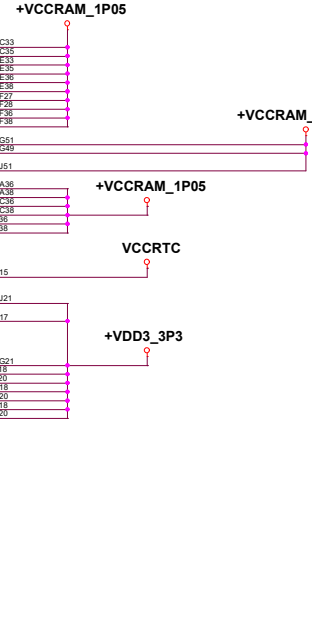
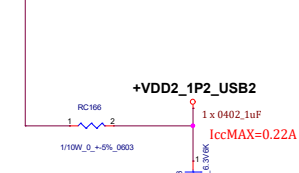
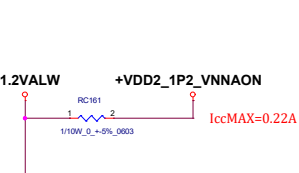
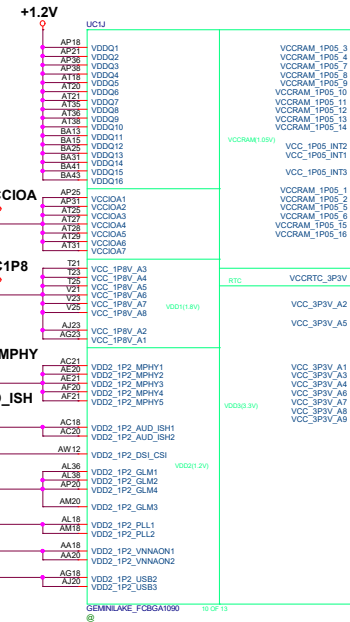
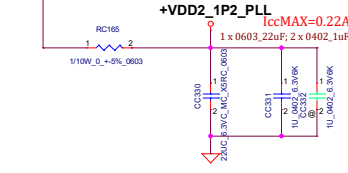
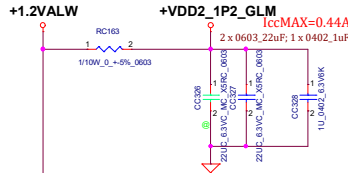
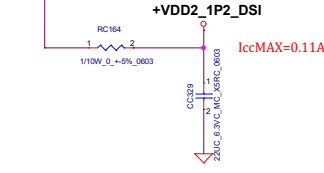
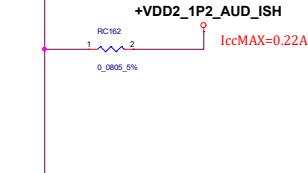
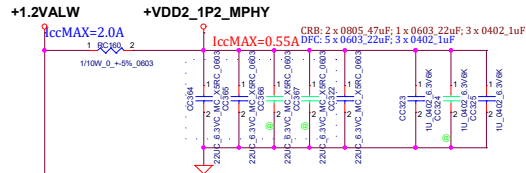
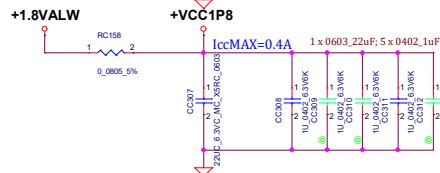
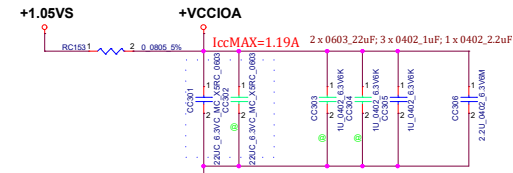
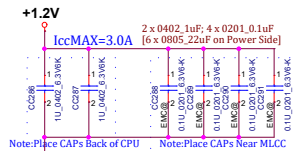


LAN WAKE



USB OCP





ccMAX=25.0A

16 x 0402_1uP


Follow Intel CRB

Follow Intel CRB

Follow CRB, Need EMC Team Confirmation

U11			
AA28	VCC_VCG1	VNN1	AF35
AA31	VCC_VCG2	VNN2	AG27
AA33	VCC_VCG3	VNN3	AG28
AE28	VCC_VCG4	VNN4	AG36
AG31	VCC_VCG5	VNN5	AG46
AE28	VCC_VCG6	VNN6	AG48
AE29	VCC_VCG7	VNN7	AJ27
AE31	VCC_VCG8	VNN8	AJ28
AF31	VCC_VCG9	VNN9	AJ46
AF33	VCC_VCG10	VNN10	AJ48
AG31	VCC_VCG11	VNN11	AL27
AG33	VCC_VCG12	VNN11	AL28
AJ31	VCC_VCG13	VNN12	AL48
AJ33	VCC_VCG14	VNN13	AL49
AJ35	VCC_VCG15	VNN14	AM27
AL31	VCC_VCG16	VNN15	AM28
AL33	VCC_VCG17	VNN16	
AL35	VCC_VCG18		
AM33	VCC_VCG19		
AM35	VCC_VCG20		
AM36	VCC_VCG21		
D31	VCC_VCG22		
D33	VCC_VCG23		
D37	VCC_VCG24		
D39	VCC_VCG25		
P39	VCC_VCG26		
P41	VCC_VCG27		
T28	VCC_VCG28		
T29	VCC_VCG29		
T31	VCC_VCG30		
T33	VCC_VCG31		
T35	VCC_VCG32		
T36	VCC_VCG33		
V28	VCC_VCG34		
V29	VCC_VCG35		
V31	VCC_VCG36		
V33	VCC_VCG37		
V35	VCC_VCG38		
V36	VCC_VCG39		
V28	VCC_VCG40		
V29	VCC_VCG41		
V33	VCC_VCG42		
V35	VCC_VCG43		
V36	VCC_VCG44		

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Security Classification		LC Future Center Secret Data		Title	
Issued Date	2018/07/09	Deciphered Date	2019/07/08	SOC (Power2)	
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UC1K

A3	VSS_6	AF44
A6	VSS_13	AF45
A12	VSS_1	AF47
A16	VSS_2	AF48
A20	VSS_3	AF50
A24	VSS_4	AF52
A28	VSS_5	AF53
A32	VSS_6	AF55
A36	VSS_7	AF56
A40	VSS_8	AF58
A44	VSS_9	AF59
A48	VSS_10	AF60
A51	VSS_11	AF61
A52	VSS_12	AF62
AA13	VSS_14	AF63
AA15	VSS_15	AF64
AA17	VSS_16	AF65
AA21	VSS_17	AF66
AA23	VSS_18	AF67
AA25	VSS_19	AF68
AA27	VSS_20	AF69
AA35	VSS_21	AF70
AA43	VSS_22	AF71
AA48	VSS_23	AF72
AB1	VSS_24	AF73
AB3	VSS_25	AF74
AB55	VSS_26	AF75
AC3	VSS_27	AF76
AC13	VSS_28	AF77
AC23	VSS_29	AF78
AC26	VSS_30	AF79
AC27	VSS_31	AF80
AC29	VSS_32	AF81
AF18	VSS_33	AF82
AE23	VSS_34	AF83
AE35	VSS_35	AF84
AE27	VSS_36	AF85
AE43	VSS_37	AF86
AE48	VSS_38	AF87
AF1	VSS_39	AF88
AF3	VSS_40	AF89
AF4	VSS_41	AF90
AF6	VSS_42	AF91
AF8	VSS_43	AF92
AF9	VSS_44	AF93
AF11	VSS_45	AF94
AF12	VSS_46	AF95
AF14	VSS_47	AF96
AF16	VSS_48	AF97
AF18	VSS_49	AF98
AF23	VSS_50	AF99
AF25	VSS_51	AF100
AF29	VSS_52	AF101
AF30	VSS_53	AF102
AF42	VSS_54	AF103

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UC1L

AN48	VSS_111	BC11
AN49	VSS_112	BC17
AN51	VSS_113	BC18
AN53	VSS_114	BC21
AP23	VSS_115	BC23
AP27	VSS_116	BC25
AP28	VSS_117	BC31
AP29	VSS_118	BC33
AP33	VSS_119	BC35
AP35	VSS_120	BC37
AR2	VSS_121	BC39
AR7	VSS_122	BC41
AR10	VSS_123	BC43
AR12	VSS_124	BC45
AR17	VSS_125	BC47
AR39	VSS_126	BC49
AR41	VSS_127	BC51
AR43	VSS_128	BC53
AR49	VSS_129	BC55
AT23	VSS_130	BC57
AT33	VSS_131	BC59
AT38	VSS_132	BC61
AU10	VSS_133	BC63
AU28	VSS_134	BC65
AU33	VSS_135	BC67
AL3	VSS_136	BC69
AL7	VSS_137	BC71
AL8	VSS_138	BC73
AL10	VSS_139	BC75
AL12	VSS_140	BC77
AL13	VSS_141	BC79
AL15	VSS_142	BC81
AL17	VSS_143	BC83
AL20	VSS_144	BC85
AL25	VSS_145	BC87
AW2	VSS_146	BC89
AW5	VSS_147	BC91
AW10	VSS_148	BC93
AW28	VSS_149	BC95
AW48	VSS_150	BC97
AW51	VSS_151	BC99
AW54	VSS_152	BC101
AY13	VSS_153	BC103
AY15	VSS_154	BC105
AY29	VSS_155	BC107
AY41	VSS_156	BC109
AY43	VSS_157	BC111
B2	VSS_158	BC113
B55	VSS_159	BC115
BA27	VSS_160	BC117
BA29	VSS_161	BC119
BB1	VSS_162	BC121
BB28	VSS_163	BC123
BB55	VSS_164	BC125
BC5	VSS_178	BC127

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UC1M

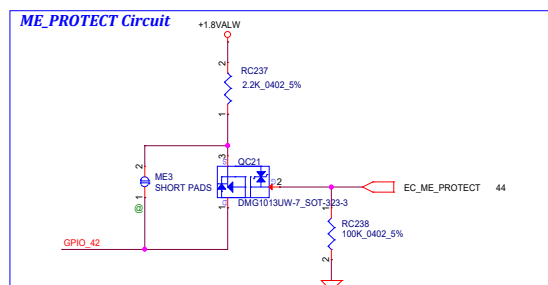
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BJ54	VSS_222	VSS_272
BK1	VSS_223	VSS_273
BK17	VSS_224	VSS_274
BK21	VSS_225	VSS_275
BK35	VSS_226	VSS_276
BK39	VSS_227	VSS_277
BK55	VSS_228	VSS_278
BL5	VSS_229	VSS_279
BL10	VSS_230	VSS_280
BL14	VSS_231	VSS_281
BL24	VSS_232	VSS_282
BL28	VSS_233	VSS_283
BL32	VSS_234	VSS_284
BL42	VSS_235	VSS_285
BL46	VSS_236	VSS_286
BL50	VSS_237	VSS_287
BL54	VSS_238	VSS_288
C1	VSS_239	VSS_289
C12	VSS_240	VSS_290
C16	VSS_241	VSS_291
C28	VSS_242	VSS_292
C36	VSS_243	VSS_293
D6	VSS_244	VSS_294
D9	VSS_245	VSS_295
D21	VSS_246	VSS_296
D28	VSS_247	VSS_297
D41	VSS_248	VSS_298
D45	VSS_249	VSS_299
D55	VSS_250	VSS_300
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E50	VSS_252	VSS_302
E55	VSS_253	VSS_303
F4	VSS_254	VSS_304
F21	VSS_255	VSS_305
F31	VSS_256	VSS_306
G28	VSS_257	VSS_307
H13	VSS_258	VSS_308
H15	VSS_259	VSS_309
H21	VSS_260	VSS_310
H23	VSS_261	VSS_311
H25	VSS_262	VSS_312
H33	VSS_263	VSS_313
H39	VSS_264	VSS_314
J8	VSS_265	VSS_315
J27	VSS_266	VSS_316
J33	VSS_267	VSS_317
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	VSS_270	VSS_320
	VSS_271	VSS_321

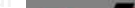
GEMINILAKE_FCBGA1090 13 OF 13

Eletr-XTechnical

Eletr-XTechnical

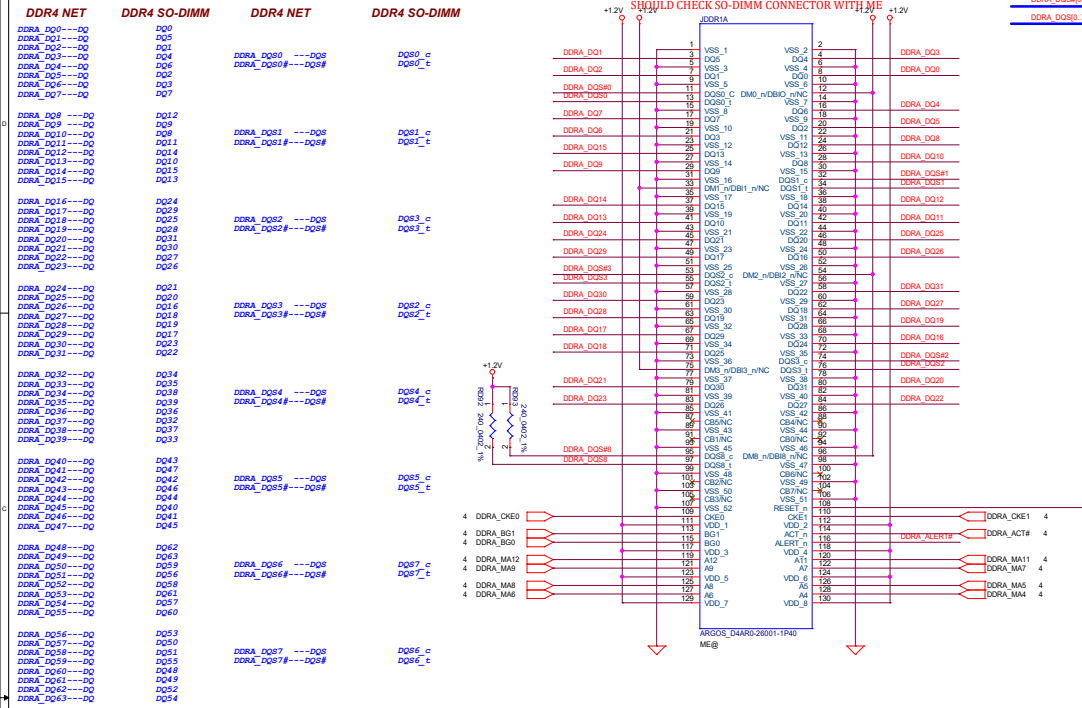
+1.8VALW



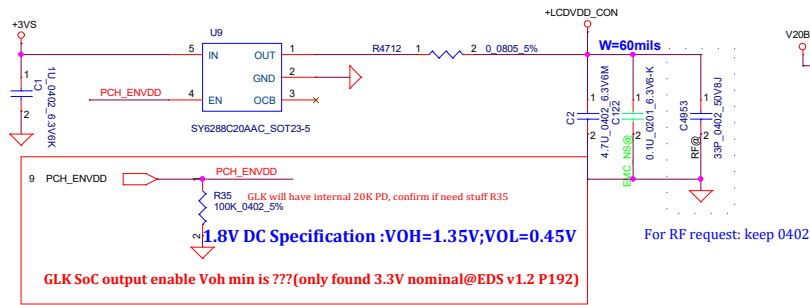
LC Future Center Secret Data		SOC (Power2)			
2018/07/09	Deciphered Date	2019/07/08			
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				FS440/FS541	0.2
			Date	Monday, November 19, 2018	

DDR4 Swap Mapping table

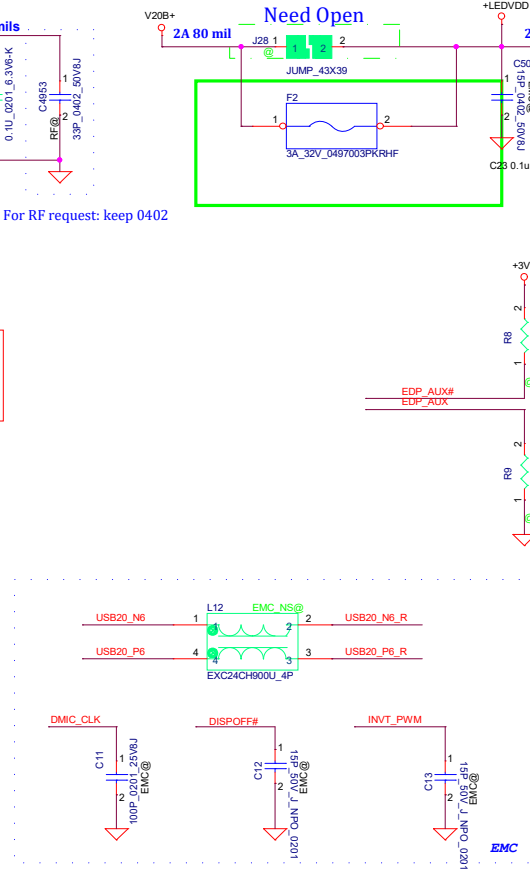
DDR4 SO-DIMM



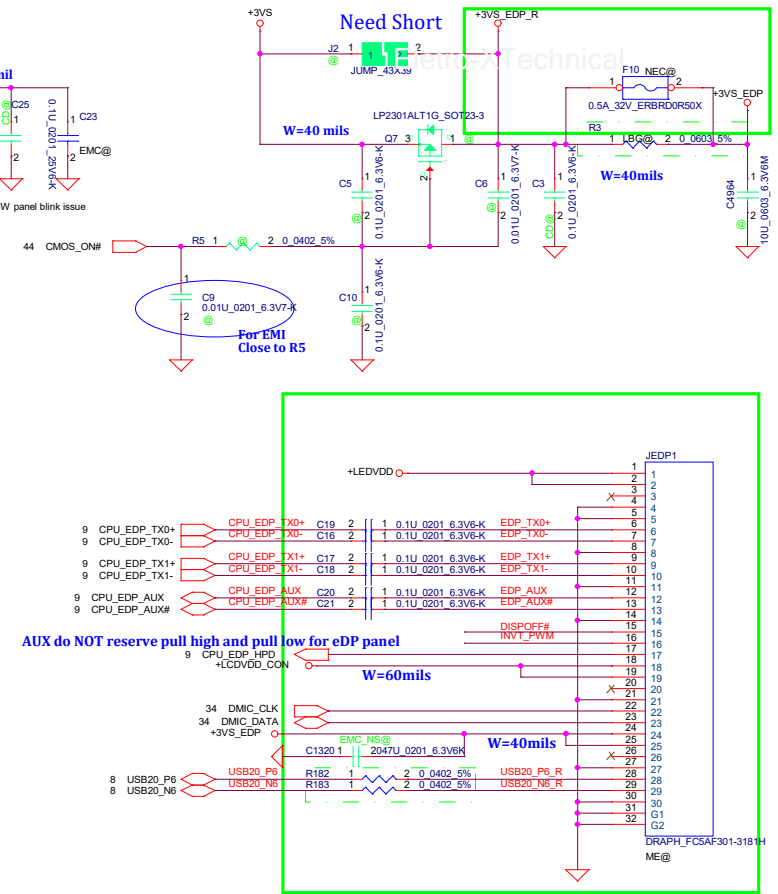
LCD POWER CIRCUIT



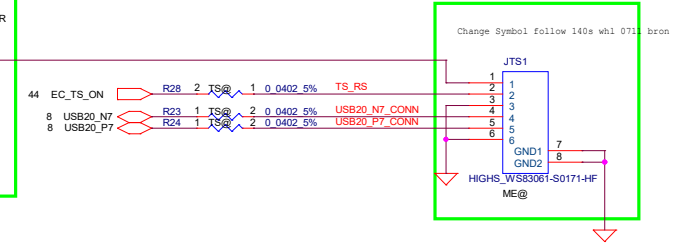
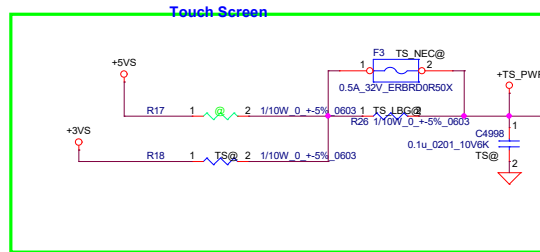
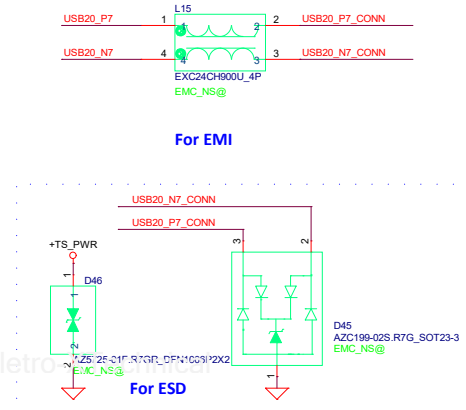
B+ to +LEDVDD POWER



CMOS CAMERA

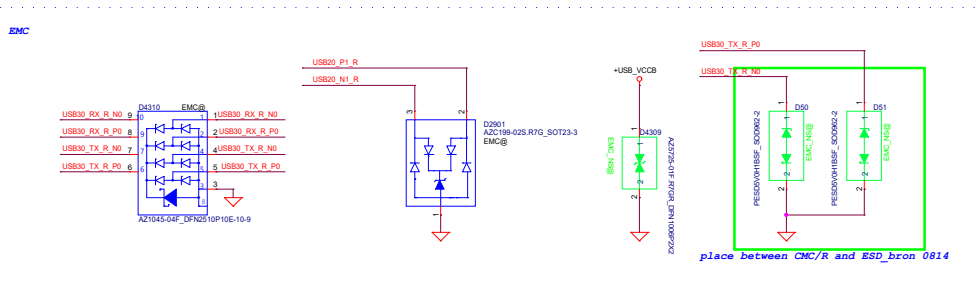
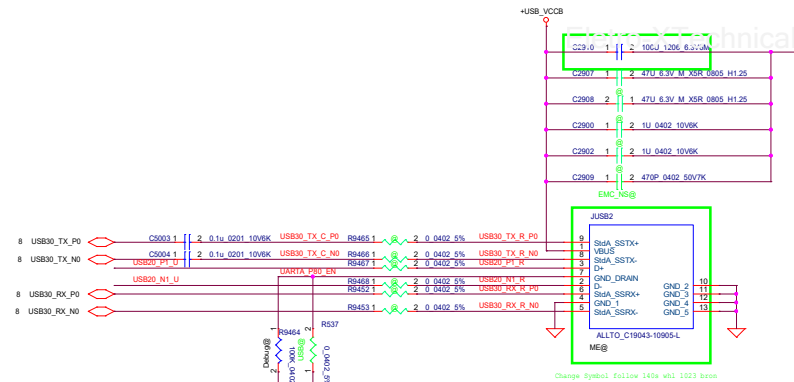
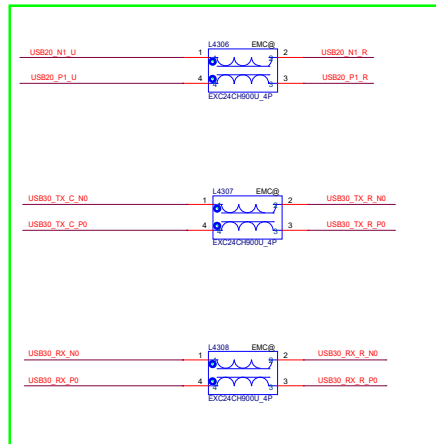
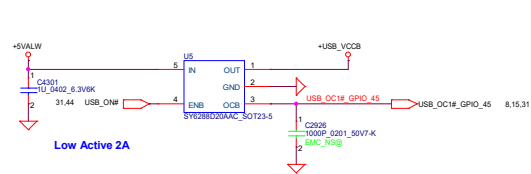


Touch Screen

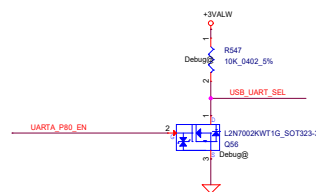
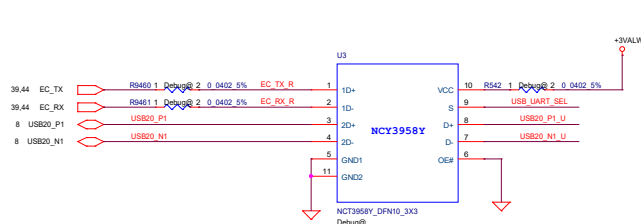


Security Classification				LC Future Center Secret Data				TITC			
Issued Date				2018/07/09				Deciphered Date			
2018/07/09				2019/07/08				eDP/CMOS			
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				Custom				FS440/FS541			
				Date				Monday, November 05, 2018			
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								Rev			
								0.2			

RIGHT SIDE USB3.0 PORT



For USB Debug Function

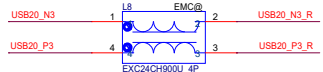
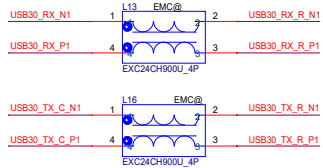
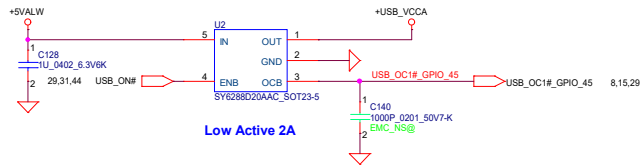


USBDEBUG	Kernel debug
Set input	Set input
Set output Low	ENABLE

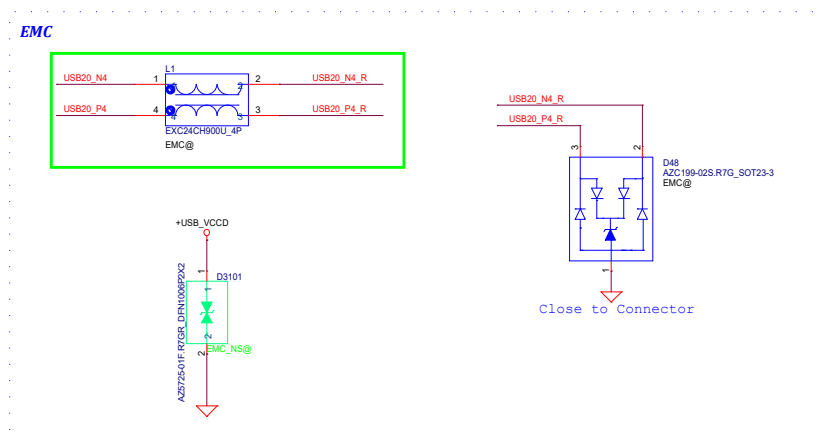
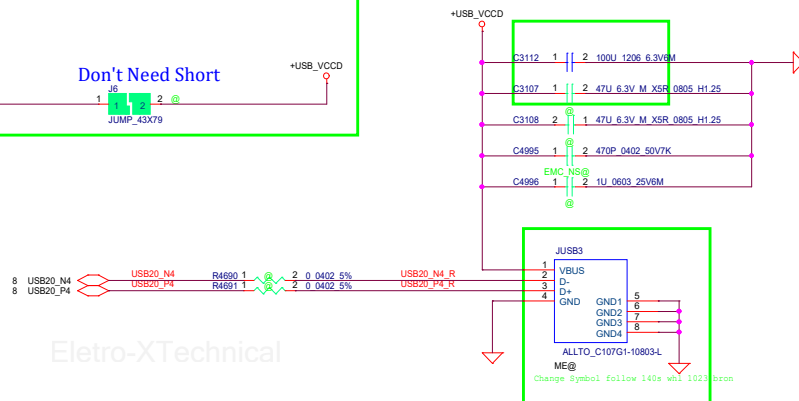
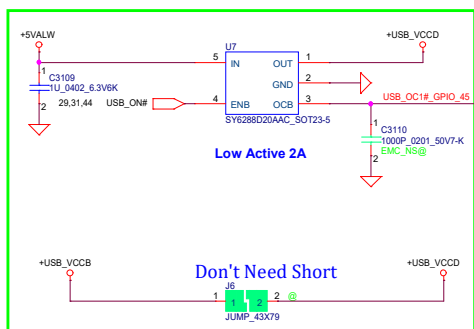
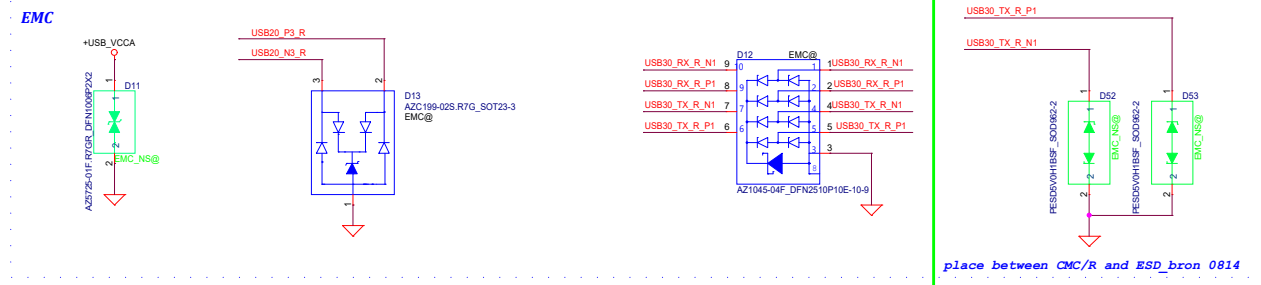
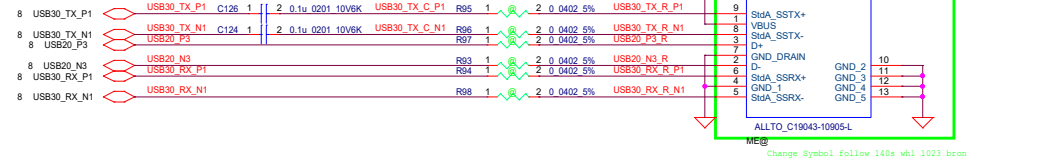
UARTA_P80_EN	POST 80
Set input	DISABLE
Set output Low	ENABLE


OE#	S	FUNCTION
H	X	DISABLE
L	L	D(+/-) to 1D(+/ -)
L	H	D(+/-) to 2D(+/ -)

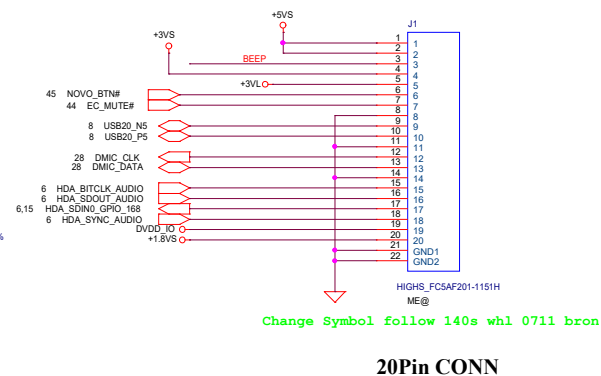
LEFT SIDE USB3.0 PORT x1




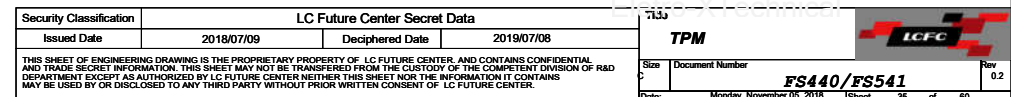
EMC



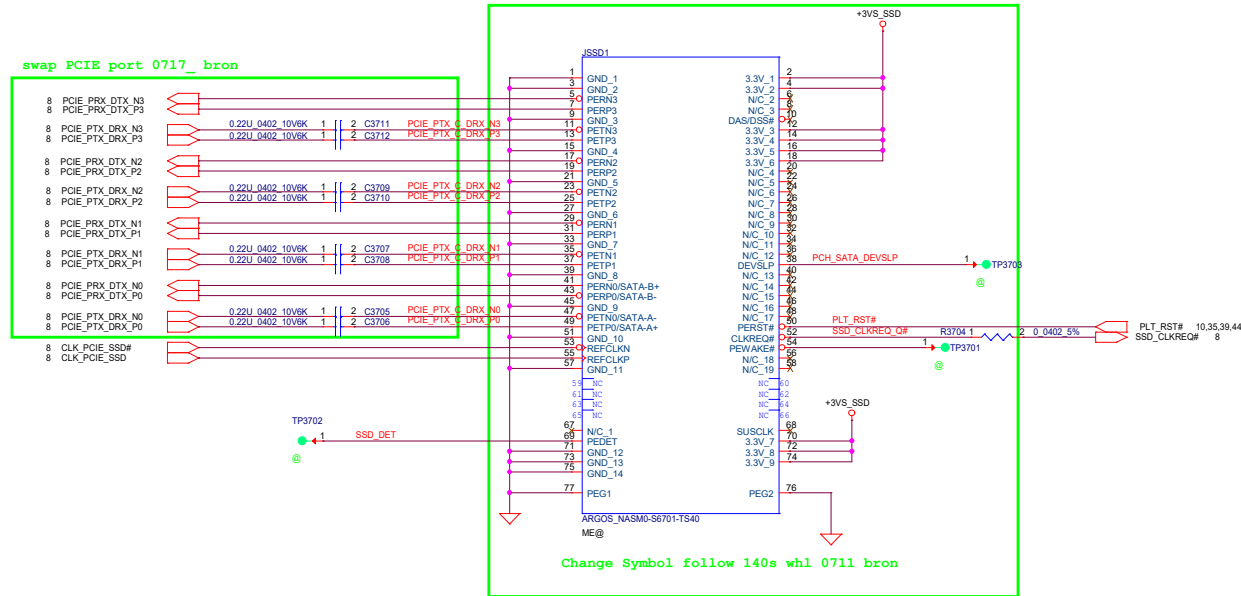
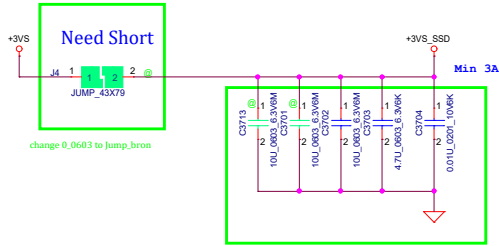
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Issued Date	2018/07/09	Deciphered Date	2019/07/08	USB3.0&USB2.0 CONN. 	
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				Date Monday, November 05, 2018 Sheet 31 of 60	



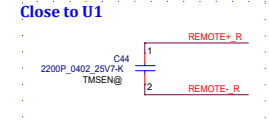
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Issued Date		2018/07/09	Deciphered Date		2019/07/08	Codec & CR_RTS5199	
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						Date: Monday, November 05, 2018 Sheet 34 of 60	



Pin No	TCG PTP Spec (v38)	Infineon SLB9670VQ2.0 FW 7.61	ST Micro ST33HTPH2E32AHB4	Nuvoton NPCT750LABYX	NATIONZ Z3H330TC
1	VDD	NC/VDD	NC	VS_B	VDD
2	GND	GND	GND	NC	GND
3	GPIO	NC	NC	NC	NC
4	GPIO	NC	NC	PP/GPIO6	NC
5	NC	NC	NC	NC	NC
6	VNC/GPIO	GPIO	GPIO	GPIO3	NC
7	GPIO/VDD	PP	PP	NC	PP
8	VDD	VDD	NC	VHIO	VDD
9	GND	GND	NC	NC	GND
10	VNC	NC	NC	NC	NC
11	NC	NC	NC	NC	NC
12	NC	NC	NC	NC	NC
13	VNC/GPIO	NC	NC	GPIO4	NC
14	VDD	NC/VDD	NC	NC	VDD
15	NC	NC	NC	NC	NC
16	GND	NC/GND	NC	GND	GND
17	SPI_RST#	RST#	SPI_RST#	PLTRST#	SPI_RST#
18	SPI_PIRQ#	PIRQ#	SPI_PIRQ#	PIRQ#/GPIO2	SPI_PIRQ#
19	SPI_CLK	SCLK	SPI_CLK	SCLK	SPI_CLK
20	SPI_CS#	CS#	SPI_CS#	SCS#/GPIO5	SPI_CS#
21	MOSI	MOSI	MOSI	MOSI/GPIO7	MOSI
22	VDD	VDD	VPS	VHIO	VDD
23	GND	GND	NC	GND	GND
24	MISO	MISO	MISO	MISO	MISO
25	NC	NC	NC	NC	NC
26	NC	NC	NC	NC	NC
27	NC	NC	NC	NC	NC
28	NC	NC	NC	NC	NC
29	VNC/GPIO	NC	NC	SDA/GPIO0	NC
30	VNC/GPIO	NC	NC	SCL/GPIO1	NC
31	VNC	NC	NC	NC	NC
32	GND	GND	NC	NC	GND



THERMAL SENSOR

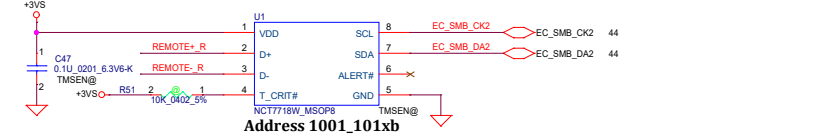


Set Thermal Sensor as a BOM Structure

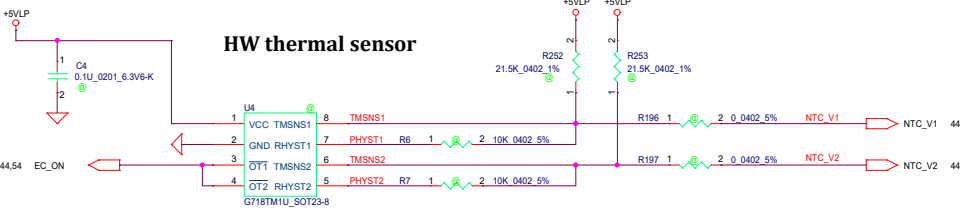


REMOTE+/-R, REMOTE1+/-, REMOTE2+/-:
Trace width/space:10/10 mil
Trace length:<8"

SMSC thermal sensor placed near DIMM

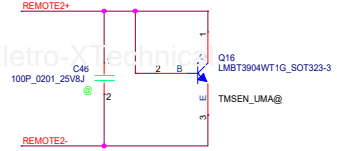


HW thermal sensor

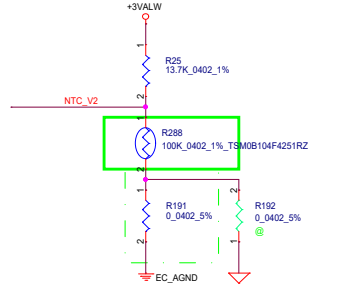


Over temperature threshold:
RSET=3*RTMH
92+/-30C
Hysteresis temperature threshold.
RHYST=(RSET*RTML)/(3*RTML-RSET)
56+/-30C

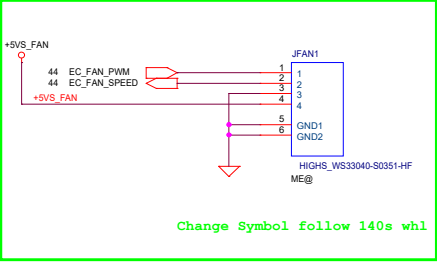
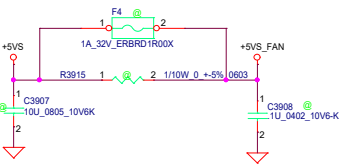
Near CPU Core



Near CPU

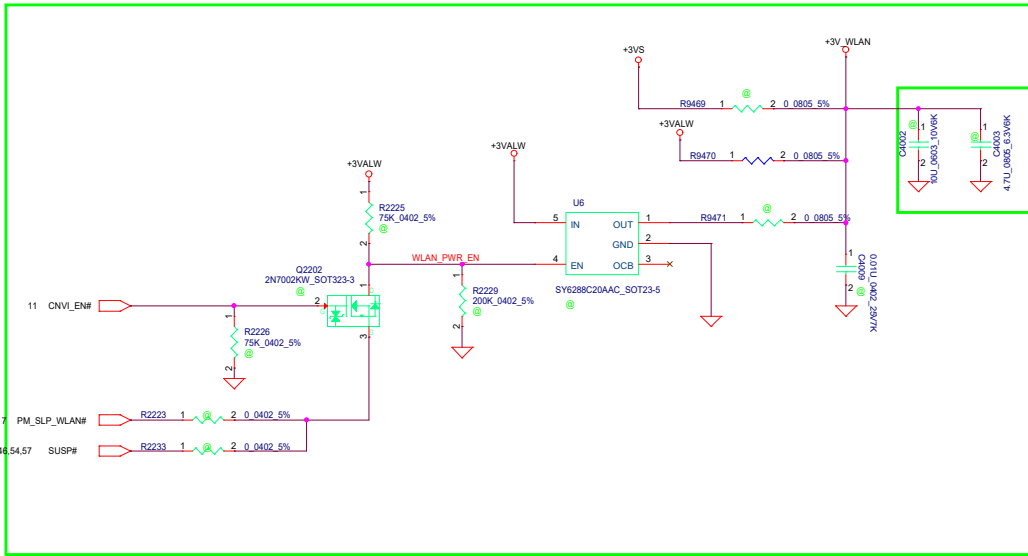


FAN Conn

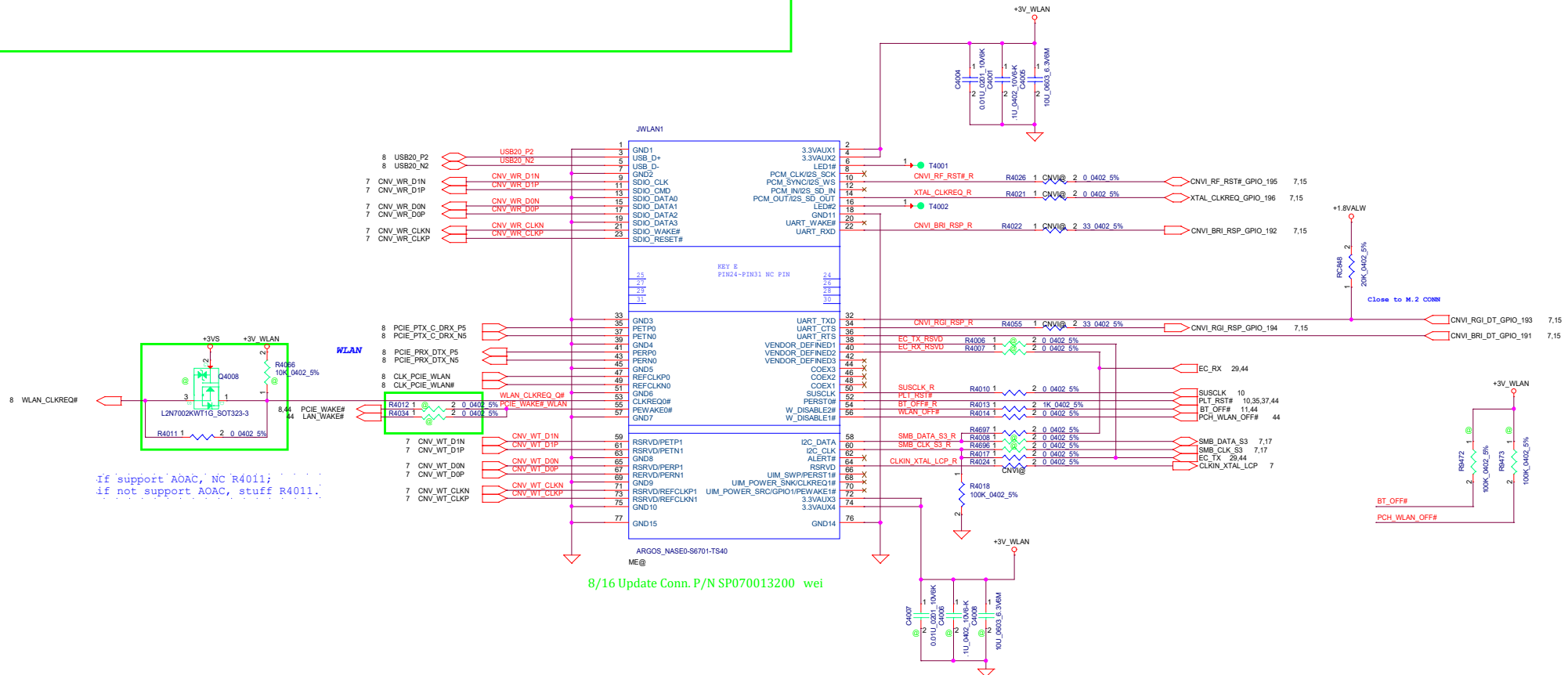
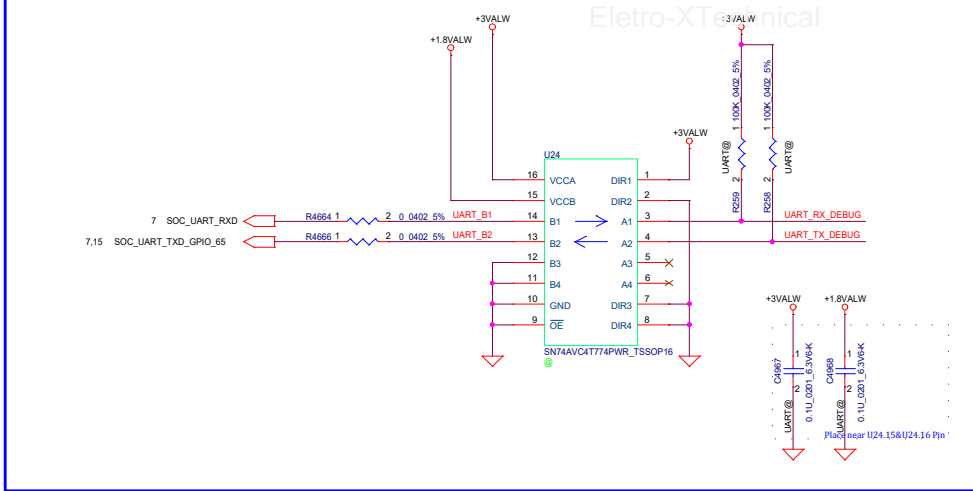


Change Symbol follow 140s whl 0711 bron

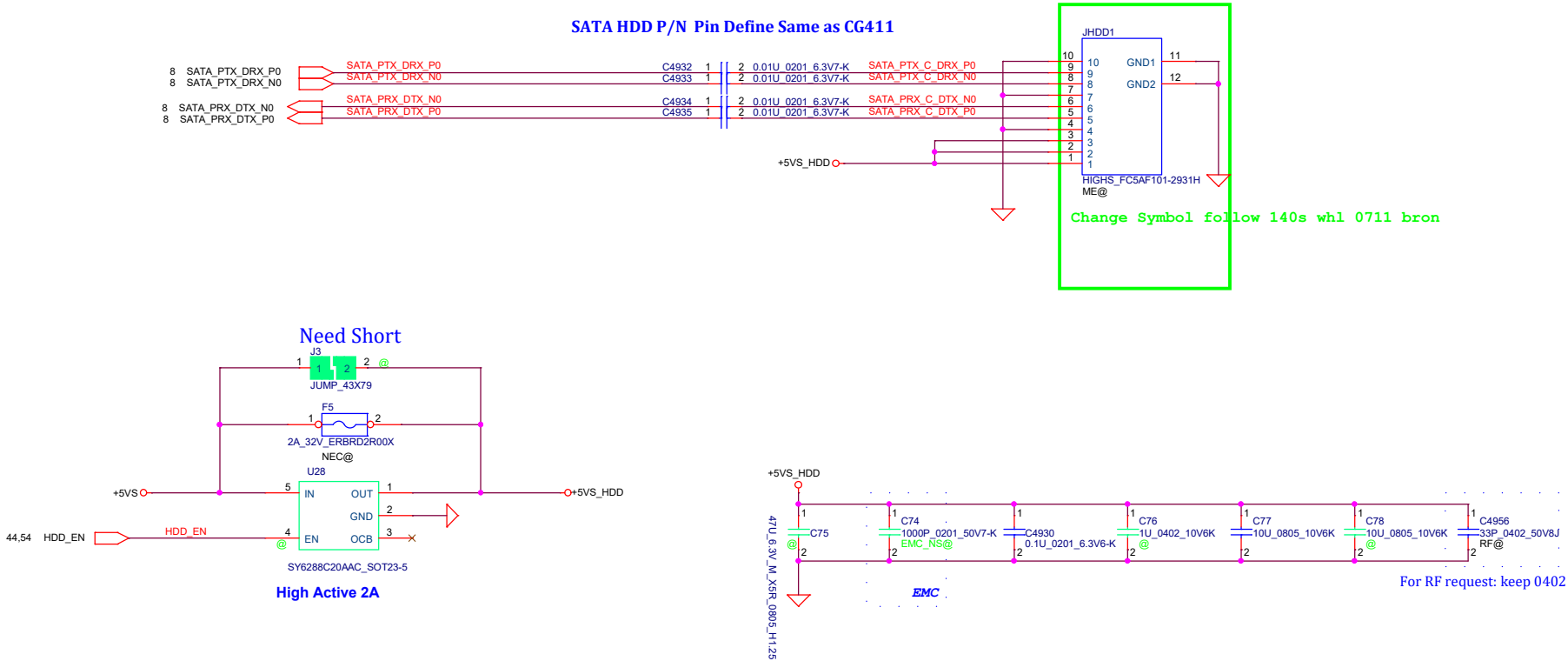
Mini-Express Card(WLAN/WiMAX)

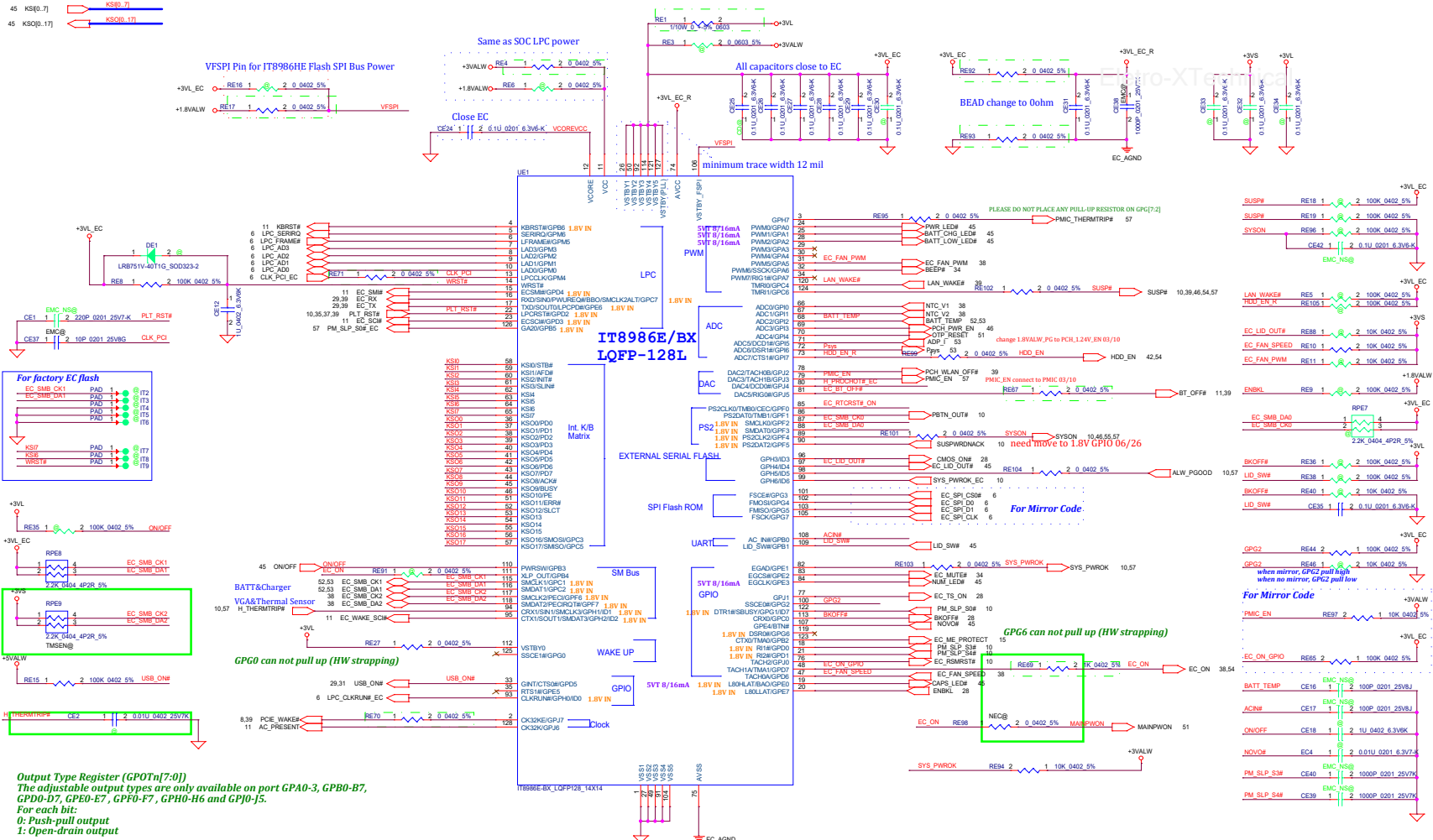


UART Transceiver

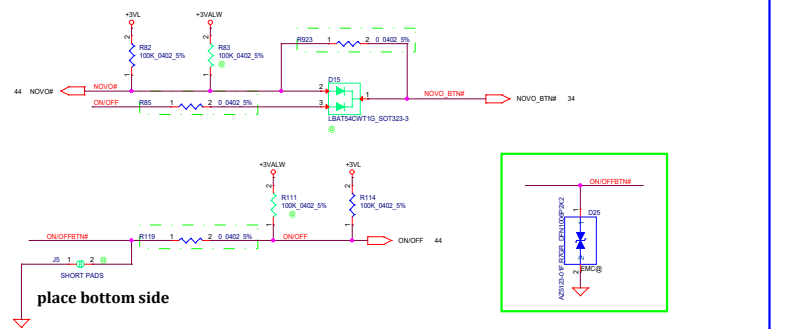


SATA HDD Conn.

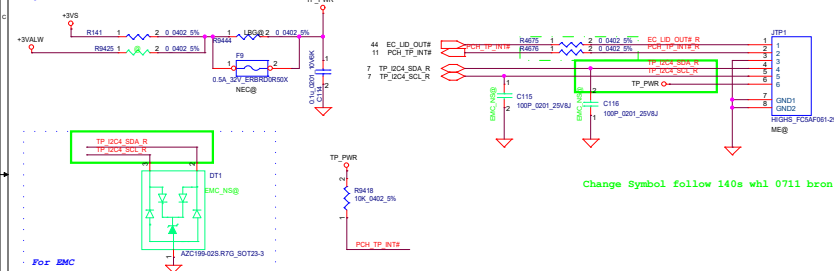




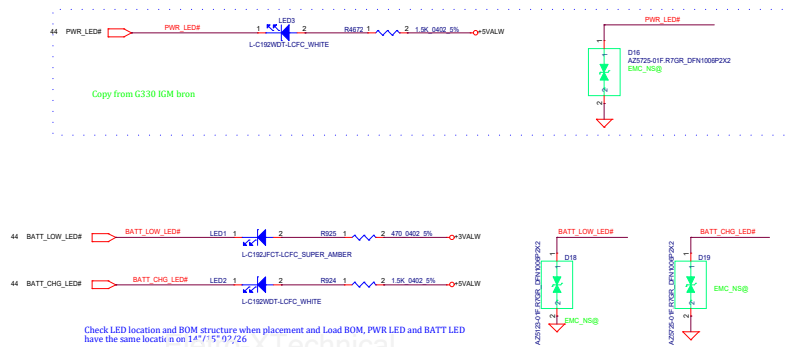
ON/OFF switch



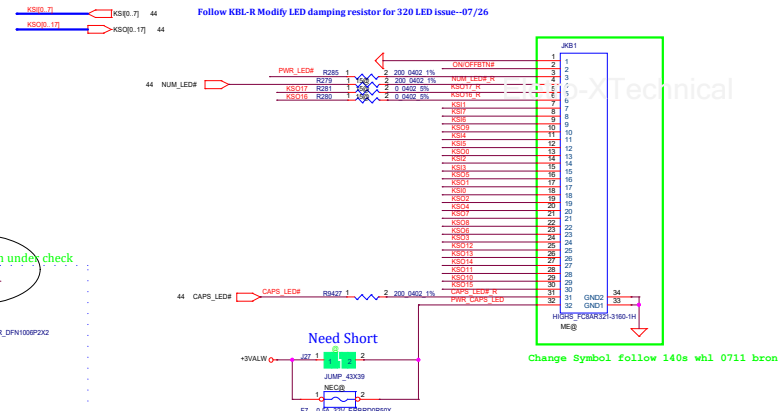
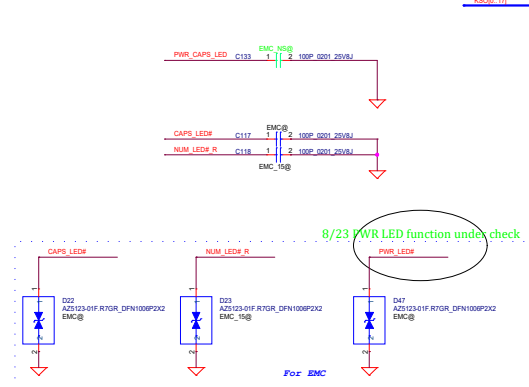
TP/B Connector



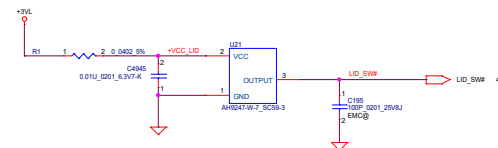
LED



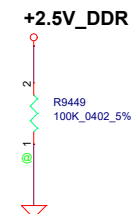
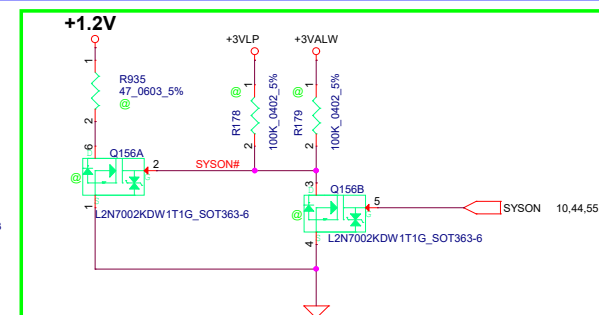
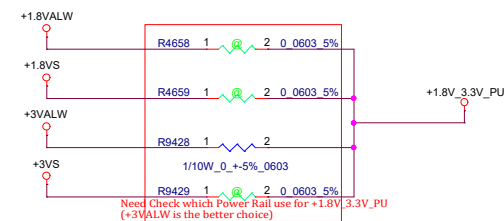
K/B Connector



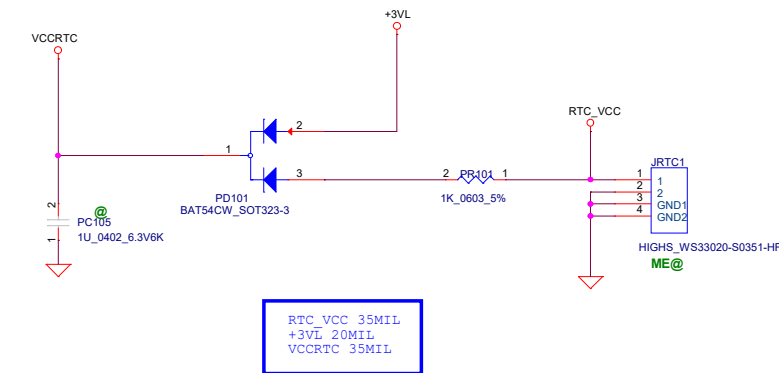
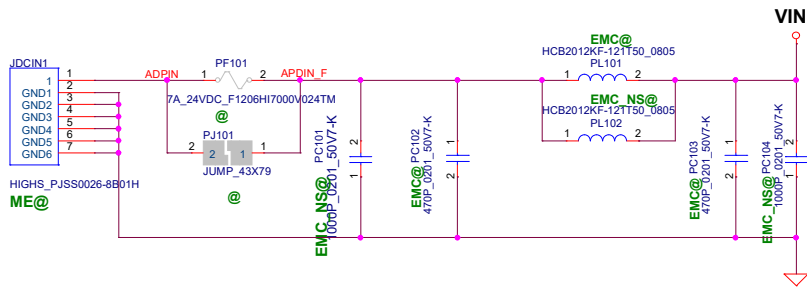
LID Switch



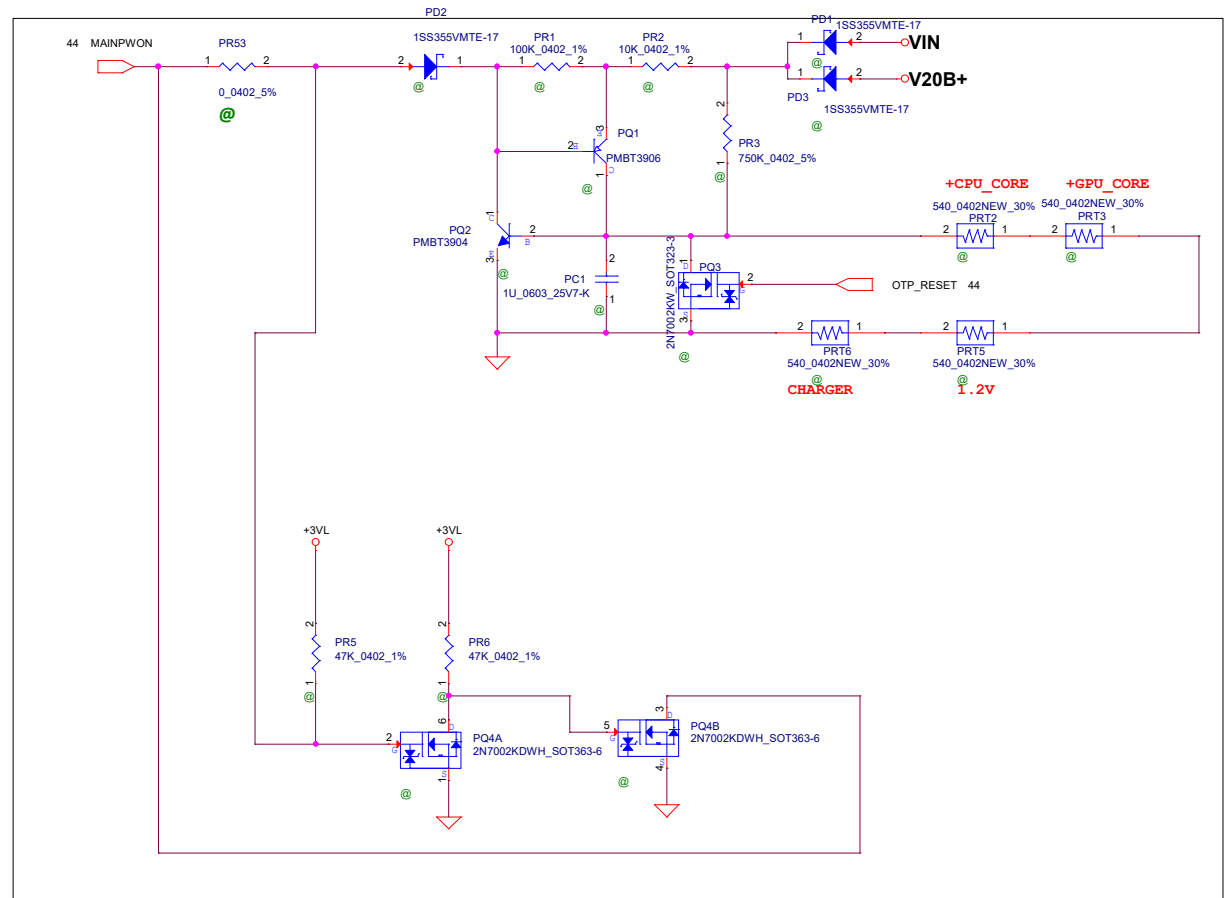
+1.8V_3.3V_PU Power Rail for 1.8/3.3 Select by Soft Strap

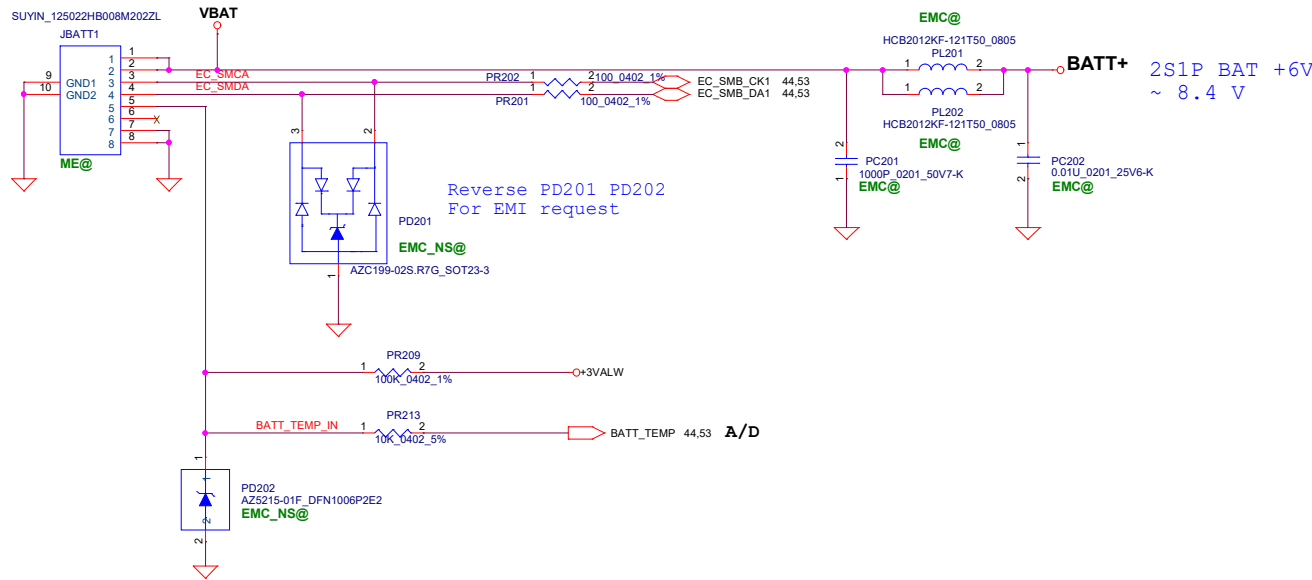


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Size	FS440/FS541				
Custom					

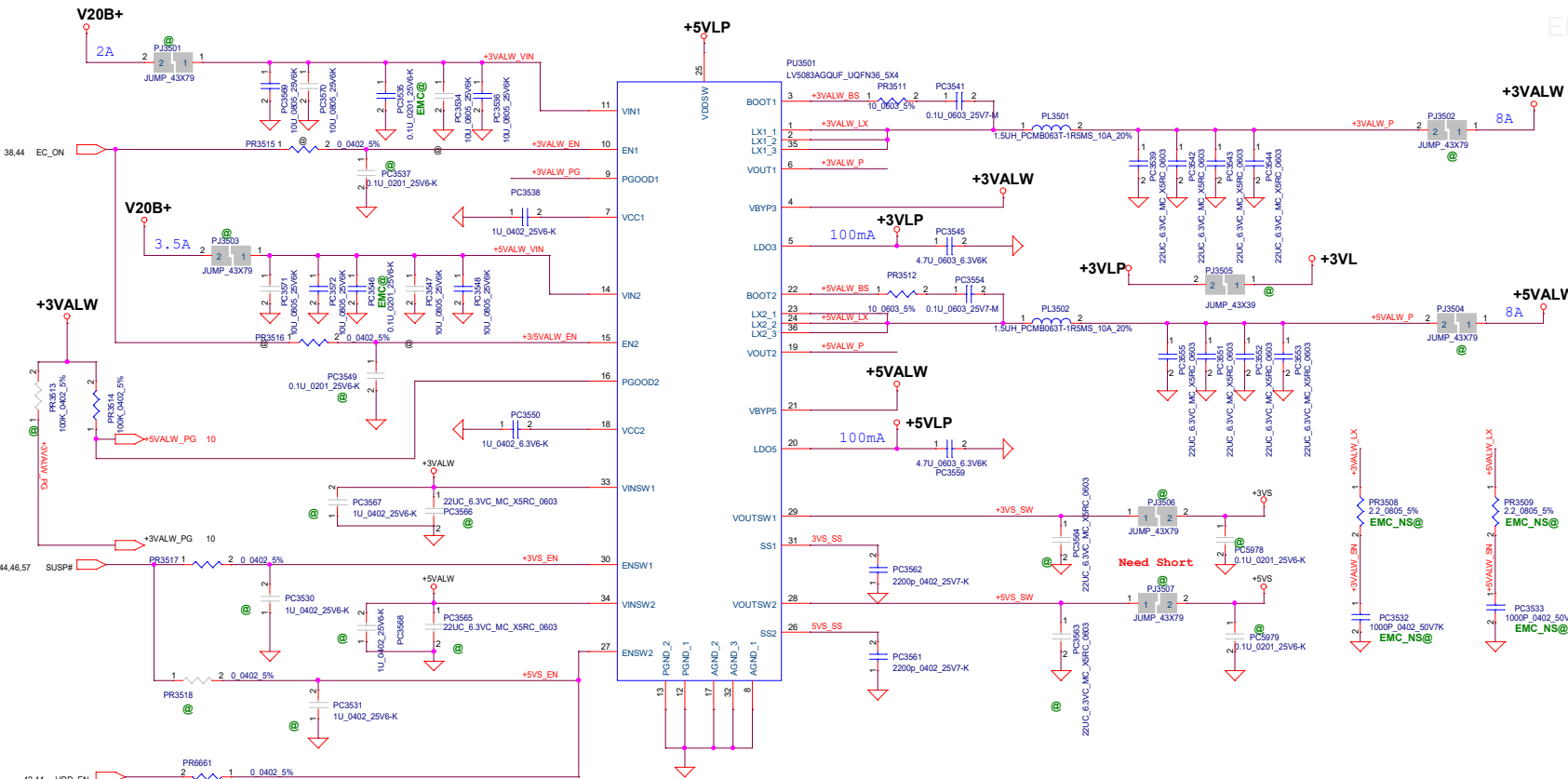


OTP



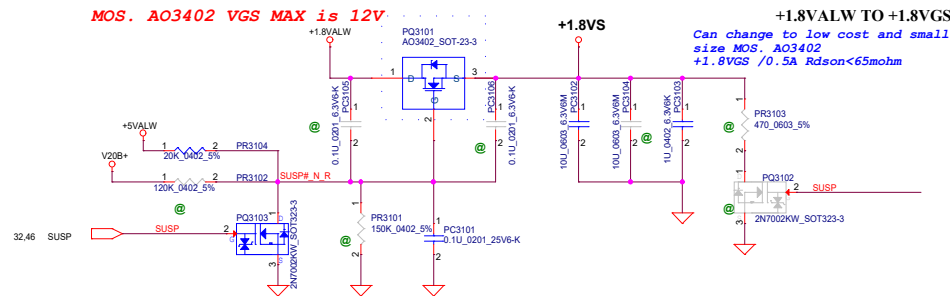






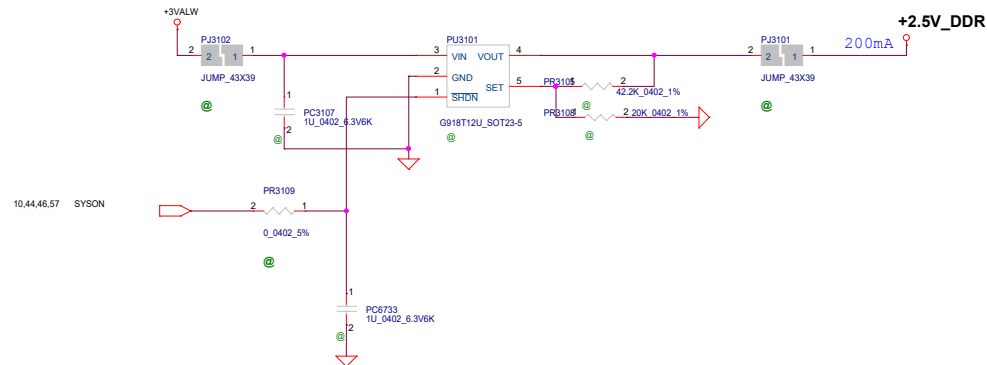
Vout=3.3V±5%
Vset=3.37V±1.5%
OCP=12A
OVP=(1.15~1.25)*Vout
UVP=(0.55~0.65)*Vout
Fsw=500Khz

Vout=5V±3%
Vset=5.1V±1.5%
OCP=12A
OVP=(1.15~1.25)*Vout
UVP=(0.55~0.65)*Vout
Fsw=500Khz




Eletro-XTechnical

RT5077A Test high temperature must add this solution
SDV Must Add in bom




Eletro-XTechnical

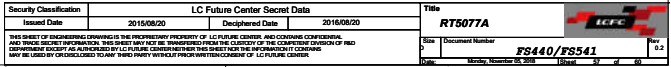
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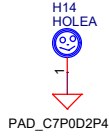
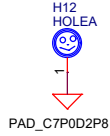
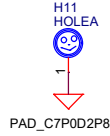
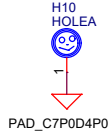
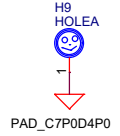
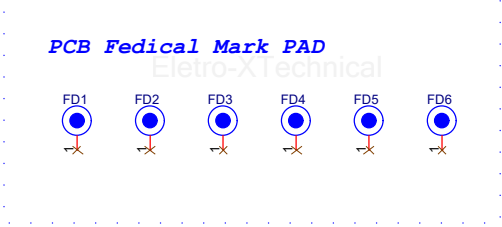
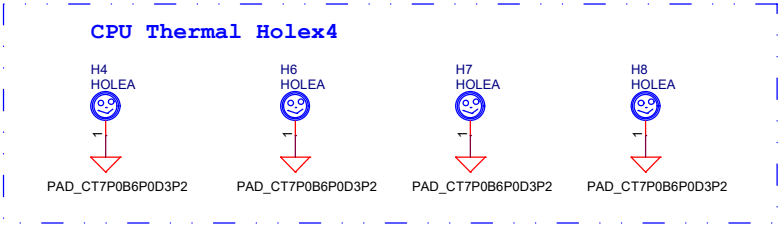
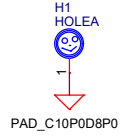
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		FS440/FS541								0.2	
Date:		Monday, November 05, 2016						Sheet		55 of 60	

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Issued Date	2015/08/20	Deciphered Date	2016/08/20	RT5077A	
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				FS440/FS541	
Date				Monday, November 05, 2018	Sheet 56 of 60

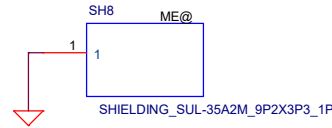
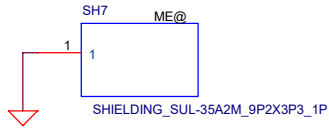
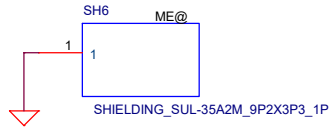
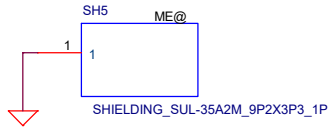
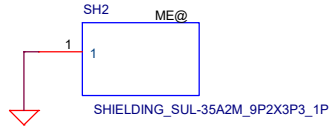
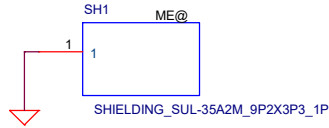


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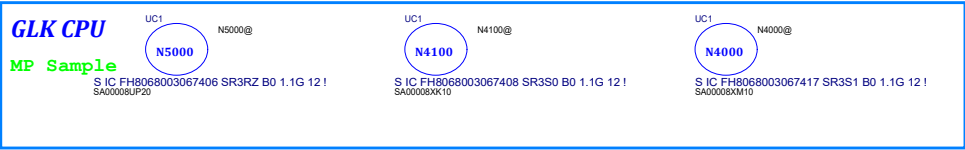
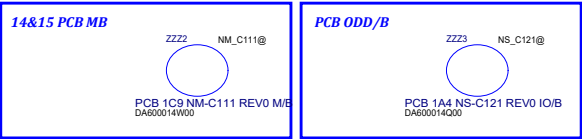


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20161216:SDV to SIT
1.p56-p57 add R=100ohm,C=680pF in FB pin;
2.pr3324 change to 55.4kohm,pr3323 change to 24.3k;
3.VNN pr3430 from 0ohm change to 20ohm, pr3428 from 210 change to 249ohm,pr3410 from 34k to 35.7k;
4.Vcore pr3330 from 0ohm change to 20ohm, pr3328 change from 287ohm to 402ohm,pr3327 change from 28.7k to 23.2k, pr3304 change from 24k to 30k;
5. GPU change 14 items to support AMD request.

20161219:SDV to SIT
1.DEL 8pcs MLCC for VNN test result.(PC3422,PC3426,PC3434,PC3436,PC3437,PC3432,PC3435,PC3433)

20161226:SDV to SIT
1. PMIC change 1.24V Vin from 3VALW to1.8VALW;
2.change PR2431 from PX@ to @, PR2433 from @ to PX@,
3.change PR734 to @.

20170104:SDV to SIT
1. PMIC change LV5075B TO LV5075A

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